EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	1	11/022154	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:16
L3	1593	segment and data and byte and (link or path) and alignment and multiplex and (buffer or storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:28
L4	1418	3 and (@rlad<"20030131" or @ad<"20030131" or @ptad<"20030131")	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 14:08
L5	716	4 and ((frequency or bandwidth) same rate)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:29
L6	24	5 and (single with (read and write) adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:30
L7	1	6 and (align$).ab.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:25
L8	12186	segment and data and byte and (link or path) and align$7 and (buffer or storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:32
L9	10405	8 and (@rlad<"20030131" or @ad<"20030131" or @ptad<"20030131")	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:33
L10	51	9 and (scal$5 with ((frequency or bandwidth) same rate))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:33
L11	0	10 and (single with (read and write) adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:30
L12	0	10 and ((read and write) adj port)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:30

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L13	45	10 and ((read and write))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:33
L14	2212	segment and data and byte and (link or path) and ((align$7) near data) and (buffer or storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:32
L15	69	segment and data and byte and (link or path) and ((align$7) near data).ab. and (buffer or storage)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:32
L16	19	15 and (((frequency or bandwidth) same rate))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:33
L17	9	16 and ((read and write))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 10:33
L18	5	17 and (@rlad<"20030131" or @ad<"20030131" or @ptad<"20030131")	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 13:04
L19	1	hypertranspot and "spi-4"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 13:08
L20	1	10/684998	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 13:11
L21	397	(spi or system adj packet adj interface) and (hypertransport or ht)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 13:12
L22	163	21 and align$6	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 13:12
L23	7	21 and (data same align$6).ab.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 13:20
L24	1	10/685231	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 13:20

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L25	259	21 and (@rlad<"20030131" or @ad<"20030131" or @ptad<"20030131")	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 13:33
L26	0	25 and aligner	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 13:33
L27	113	25 and align$6	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 13:33
L28	45	25 and data with align$6	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 13:34
L29	8	28 and "370"/$.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2007/10/24 13:58

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Date: 10/24/2007

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Time: 13:30:35

Inventor Information for 10/685231

Inventor Name	City	State/Country
GULATI, MANU	SAN FRANCISCO	CALIFORNIA
MOLL, LAURENT R.	SARATOGA	CALIFORNIA

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Inventor Name Search Result

Your Search was:

Last Name = GULATI
First Name = MANU

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09137583	6175911	150	08/21/1998	METHOD AND APPARATUS FOR CONCURRENTLY EXECUTING MULTIPLICATION AND ITERATIVE OPERATIONS	GULATI, MANU
09385186	Not Issued	161	08/30/1999	APPARATUS AND METHOD FOR MAINTAINING AN ARCHITECTURAL STATUS REGISTER	GULATI, MANU
10269666	6912602	150	10/11/2002	SYSTEM HAVING TWO OR MORE PACKET INTERFACES, A SWITCH, AND A SHARED PACKET DMA CIRCUIT	GULATI, MANU
10269922	7206879	150	10/11/2002	SYSTEMS USING MIX OF PACKET, COHERENT, AND NONCOHERENT TRAFFIC TO OPTIMIZE TRANSMISSION BETWEEN SYSTEMS	GULATI, MANU
10270016	7227870	150	10/11/2002	SYSTEMS INCLUDING PACKET INTERFACES, SWITCHES, AND PACKET DMA CIRCUITS FOR SPLITTING AND MERGING PACKET STREAMS	GULATI, MANU
10270029	6748479	150	10/11/2002	SYSTEM HAVING INTERFACES AND SWITCH THAT SEPARATES COHERENT AND PACKET TRAFFIC	GULATI, MANU
10356321	6944719	150	01/31/2003	SCALABLE CACHE COHERENT DISTRIBUTED SHARED MEMORY PROCESSING SYSTEM	GULATI, MANU
10356323	Not	71	01/31/2003	Efficient routing of packet data in	GULATI, MANU

	Issued			a scalable processing resource	
10356324	Not Issued	71	01/31/2003	Processing of received data within a multiple processor device	GULATI, MANU
10356346	Not Issued	30	01/31/2003	Bandwidth allocation fairness within a processing system of a plurality of processing devices	GULATI, MANU
10356348	Not Issued	61	01/31/2003	Transmitting data from a plurality of virtual channels via a multiple processor device	GULATI, MANU
10356390	Not Issued	61	01/31/2003	Multiple processor integrated circuit having configurable packet-based interfaces	GULATI, MANU
10356661	Not Issued	41	01/31/2003	Packet data service over hyper transport link(s)	GULATI, MANU
10421988	Not Issued	41	04/23/2003	Smart routing between peers in a point-to-point link based system	GULATI, MANU
10439297	6941440	150	05/15/2003	ADDRESSING SCHEME SUPPORTING VARIABLE LOCAL ADDRESSING AND VARIABLE GLOBAL ADDRESSING	GULATI, MANU
10675745	Not Issued	71	09/30/2003	Management of received data within host device using linked lists	GULATI, MANU
10684915	7272151	150	10/14/2003	CENTRALIZED SWITCHING FABRIC SCHEDULER SUPPORTING SIMULTANEOUS UPDATES	GULATI, MANU
10684989	Not Issued	93	10/14/2003	TRANSPARENT DATA FORMAT WITHIN HOST DEVICE SUPPORTING DIFFERING TRANSACTION TYPES	GULATI, MANU
10684998	Not Issued	93	10/14/2003	APPARATUS AND METHOD TO RECEIVE AND DECODE INCOMING DATA AND TO HANDLE REPEATED SIMULTANEOUS SMALL FRAGMENTS	GULATI, MANU
10685231	Not Issued	30	10/14/2003	Apparatus and method to receive and align incoming data in a buffer to expand data width by utilizing a single write port memory device	GULATI, MANU
10742060	Not Issued	41	12/20/2003	Hypertransport/SPI-4 interface supporting configurable deskewing	GULATI, MANU

10861624	6941406	150	06/04/2004	SYSTEM HAVING INTERFACES AND SWITCH THAT SEPARATES COHERENT AND PACKET TRAFFIC	GULATI, MANU
11069313	Not Issued	30	03/01/2005	System having two or more packet interfaces, a switch, and a shared packet DMA circuit	GULATI, MANU
11146449	Not Issued	30	06/07/2005	System having interfaces and switch that separates coherent and packet traffic	GULATI, MANU
11146450	Not Issued	41	06/07/2005	Addressing scheme supporting variable local addressing and variable global addressing	GULATI, MANU
11182123	7171521	150	07/15/2005	COHERENT SHARED MEMORY PROCESSING SYSTEM	GULATI, MANU
11717511	Not Issued	30	03/13/2007	Systems using mix of packet, coherent, and noncoherent traffic to optimize transmission between systems	GULATI, MANU
11786275	Not Issued	30	04/11/2007	Receiving data from virtual channels	GULATI, MANU
11803637	Not Issued	25	05/15/2007	Systems including packet interfaces, switches, and packet DMA circuits for splitting and merging packet streams	GULATI, MANU
60331789	Not Issued	159	11/20/2001	Packet data service over hyper transport link(s)	GULATI, MANU
60344713	Not Issued	159	12/24/2001	Multi-function hypertransport devices	GULATI, MANU
60348717	Not Issued	159	01/14/2002	Hyper transport coupled distributed system host	GULATI, MANU
60348777	Not Issued	159	01/14/2002	Multi-function hypertransport devices	GULATI, MANU
60380740	Not Issued	159	05/15/2002	System on chip for networking	GULATI, MANU
60419031	Not Issued	160	10/16/2002	Processing of received data within a multiple processor device	GULATI, MANU
60419032	Not Issued	159	10/16/2002	Multiple processor integrated circuit having configurable packet-based interfaces	GULATI, MANU
60419033	Not Issued	159	10/16/2002	Scalable cache coherent distributed shared memory processing system	GULATI, MANU
60419040	Not	159	10/16/2002	Transmitting data from a plurality	GULATI, MANU

	Issued			of virtual channels via a multiple processor device	
60419041	Not Issued	159	10/16/2002	Packet data service over hypertransport links	GULATI, MANU
60419042	Not Issued	159	10/16/2002	Efficient routing of packet data in a scalable processing resource	GULATI, MANU
60419043	Not Issued	159	10/16/2002	Bandwidth allocation fairness within a processing system of a plurality of processing devices	GULATI, MANU
60520166	Not Issued	159	11/14/2003	Hyper transport/SPI-4 interface supporting configurable deskewing	GULATI, MANU

Inventor Search Completed: No Records to Display.

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Inventor Name Search Result

Your Search was:

Last Name = MOLL
First Name = LAURENT

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09264347	6753878	150	03/08/1999	PARALLEL PIPELINED MERGE ENGINES	MOLL, LAURENT
10356323	Not Issued	71	01/31/2003	Efficient routing of packet data in a scalable processing resource	MOLL, LAURENT
10356324	Not Issued	71	01/31/2003	Processing of received data within a multiple processor device	MOLL, LAURENT
10356348	Not Issued	61	01/31/2003	Transmitting data from a plurality of virtual channels via a multiple processor device	MOLL, LAURENT
10356390	Not Issued	61	01/31/2003	Multiple processor integrated circuit having configurable packet-based interfaces	MOLL, LAURENT
10356661	Not Issued	41	01/31/2003	Packet data service over hyper transport link(s)	MOLL, LAURENT
10684871	Not Issued	61	10/14/2003	Hash and route hardware with parallel routing scheme	MOLL, LAURENT
10684909	7131020	150	10/14/2003	DISTRIBUTED COPIES OF CONFIGURATION INFORMATION USING TOKEN RING	MOLL, LAURENT
10684915	7272151	150	10/14/2003	CENTRALIZED SWITCHING FABRIC SCHEDULER SUPPORTING SIMULTANEOUS UPDATES	MOLL, LAURENT
10684953	Not Issued	41	10/14/2003	Hypertransport exception detection and processing	MOLL, LAURENT
10685129	7243172	150	10/14/2003	FRAGMENT STORAGE FOR DATA ALIGNMENT AND MERGER	MOLL, LAURENT
10685376	7218638	150	10/14/2003	SWITCH OPERATION SCHEDULING MECHANISM WITH CONCURRENT	MOLL, LAURENT

				CONNECTION AND QUEUE SCHEDULING	
10864609	Not Issued	20	06/09/2004	Parallel pipelined merge engines	MOLL, LAURENT
10941172	Not Issued	61	09/15/2004	System and method for data transfer between multiple proccessors	MOLL, LAURENT
11781726	Not Issued	19	07/23/2007	VIRTUAL CORE MANAGEMENT	MOLL, LAURENT
11786275	Not Issued	30	04/11/2007	Receiving data from virtual channels	MOLL, LAURENT
60331789	Not Issued	159	11/20/2001	Packet data service over hyper transport link(s)	MOLL, LAURENT
60344713	Not Issued	159	12/24/2001	Multi-function hypertransport devices	MOLL, LAURENT
60348717	Not Issued	159	01/14/2002	Hyper transport coupled distributed system host	MOLL, LAURENT
60348777	Not Issued	159	01/14/2002	Multi-function hypertransport devices	MOLL, LAURENT
60419031	Not Issued	160	10/16/2002	Processing of received data within a multiple processor device	MOLL, LAURENT
60419040	Not Issued	159	10/16/2002	Transmitting data from a plurality of virtual channels via a multiple processor device	MOLL, LAURENT
60419041	Not Issued	159	10/16/2002	Packet data service over hypertransport links	MOLL, LAURENT
60419042	Not Issued	159	10/16/2002	Efficient routing of packet data in a scalable processing resource	MOLL, LAURENT
60520166	Not Issued	159	11/14/2003	Hyper transport/SPI-4 interface supporting configurable deskewing	MOLL, LAURENT
10269666	6912602	150	10/11/2002	SYSTEM HAVING TWO OR MORE PACKET INTERFACES, A SWITCH, AND A SHARED PACKET DMA CIRCUIT	MOLL, LAURENT R.
10269922	7206879	150	10/11/2002	SYSTEMS USING MIX OF PACKET, COHERENT, AND NONCOHERENT TRAFFIC TO OPTIMIZE TRANSMISSION BETWEEN SYSTEMS	MOLL, LAURENT R.
10270016	7227870	150	10/11/2002	SYSTEMS INCLUDING PACKET INTERFACES, SWITCHES, AND PACKET DMA CIRCUITS FOR SPLITTING AND MERGING	MOLL, LAURENT R.

				PACKET STREAMS	
10270029	6748479	150	10/11/2002	SYSTEM HAVING INTERFACES AND SWITCH THAT SEPARATES COHERENT AND PACKET TRAFFIC	MOLL, LAURENT R.
10439297	6941440	150	05/15/2003	ADDRESSING SCHEME SUPPORTING VARIABLE LOCAL ADDRESSING AND VARIABLE GLOBAL ADDRESSING	MOLL, LAURENT R.
10439343	Not Issued	61	05/15/2003	Addressing scheme supporting fixed local addressing and variable global addressing	MOLL, LAURENT R.
10675745	Not Issued	71	09/30/2003	Management of received data within host device using linked lists	MOLL, LAURENT R.
10684872	7096305	150	10/14/2003	PERIPHERAL BUS SWITCH HAVING VIRTUAL PERIPHERAL BUS AND CONFIGURABLE HOST BRIDGE	MOLL, LAURENT R.
10684988	Not Issued	41	10/14/2003	Peripheral bus transaction routing using primary and node ID routing information	MOLL, LAURENT R.
10684989	Not Issued	93	10/14/2003	TRANSPARENT DATA FORMAT WITHIN HOST DEVICE SUPPORTING DIFFERING TRANSACTION TYPES	MOLL, LAURENT R.
10684998	Not Issued	93	10/14/2003	APPARATUS AND METHOD TO RECEIVE AND DECODE INCOMING DATA AND TO HANDLE REPEATED SIMULTANEOUS SMALL FRAGMENTS	MOLL, LAURENT R.
10685231	Not Issued	30	10/14/2003	Apparatus and method to receive and align incoming data in a buffer to expand data width by utilizing a single write port memory device	MOLL, LAURENT R.
10742060	Not Issued	41	12/20/2003	Hypertransport/SPI-4 interface supporting configurable deskewing	MOLL, LAURENT R.
10861624	6941406	150	06/04/2004	SYSTEM HAVING INTERFACES AND SWITCH	MOLL, LAURENT R.

				THAT SEPARATES COHERENT AND PACKET TRAFFIC	
11069313	Not Issued	30	03/01/2005	System having two or more packet interfaces, a switch, and a shared packet DMA circuit	MOLL, LAURENT R.
11146449	Not Issued	30	06/07/2005	System having interfaces and switch that separates coherent and packet traffic	MOLL, LAURENT R.
11146450	Not Issued	41	06/07/2005	Addressing scheme supporting variable local addressing and variable global addressing	MOLL, LAURENT R.
11279880	Not Issued	30	04/15/2006	Improved Prefetch Hardware Efficiency via Prefetch Hint Instructions	MOLL, LAURENT R.
11351058	Not Issued	30	02/09/2006	Small and power-efficient cache that can provide data for background DMA devices while the processor is in a low-power state	MOLL, LAURENT R.
11351070	Not Issued	30	02/09/2006	Power conservation via DRAM access reduction	MOLL, LAURENT R.
11416872	Not Issued	30	05/02/2006	System and method for optimizing a memory controller	MOLL, LAURENT R.
11435528	Not Issued	30	05/17/2006	System and method for processing instructions in a computer system	MOLL, LAURENT R.
11446897	Not Issued	30	06/05/2006	Peripheral bus switch having virtual peripheral bus and configurable host bridge	MOLL, LAURENT R.
11450103	Not Issued	30	06/09/2006	System and method for conserving power	MOLL, LAURENT R.
11543549	Not Issued	30	10/04/2006	Cache instructions with hierarchy control	MOLL, LAURENT R.

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